iND880xx

Camera Video Processor

iND880xx Features

- 1400 MP/s ISP Processing throughput
- Supports up to 4 cameras and 8 video streams simultaneously
- Low latency ISP processing
- eWarp® geometric processor
- No external DRAM required
- ASIL-B compliant
- Supports HSM for cybersecurity needs
- Automotive Qualified (AECQ-100 Grade-2)

Applications

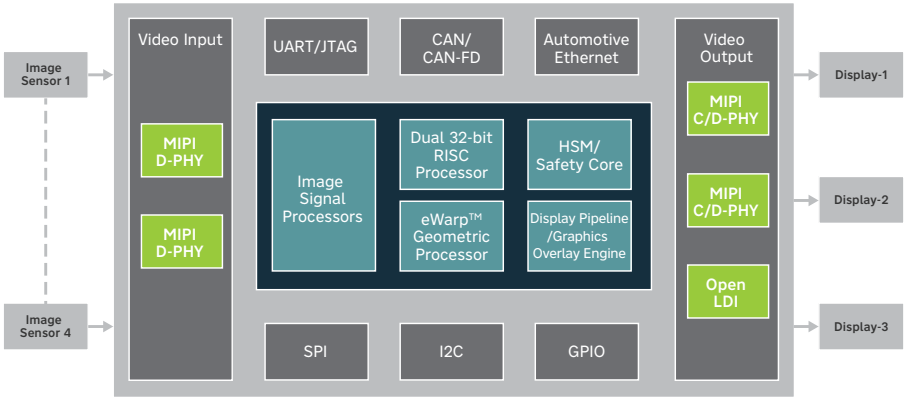
Automotive

- Single/ Multi-camera eMirror Systems
- ISP Hub for multi-camera systems
- Front camera/ECU preprocessor
- Driver and Occupant Monitoring Systems (DMS/ OMS)
- Rearview camera system
- Parking assistance camera systems

Robotics and Industrial

- Multi-sensor hub for Autonomous Mobile Robots (AMR) and Automated Guided Vehicles (AGV)
- Machine vision
- Drone vision
- 3D perception cameras
- 360-degree vision

The iND880xx family of Camera Video Processors (CVPs) deliver next generation image processing optimized for both human and computer vision while boasting sub-1ms latency from video-in to video-out. With a high dynamic range image pipeline reaching 144 dB, these processors are finely tuned for optimal performance across various Color Filter Array (CFA) configurations. iND880xx can seamlessly connect to four cameras, offering the versatility to configure and process up to eight distinct image pipelines simultaneously. Anticipating future demands in automotive, robotics, and industrial applications, these products are equipped with enhanced support for new CFAs like RGB-IR, RCCG, RYYCy, RCCC, and RCCB, along with compatibility with multiple high-resolution sensors. Moreover, incorporating a dedicated hardware security and safety engine, the iND880xx family provides customers with a scalable and adaptable platform to meet a wide array of performance requirements and sensor specifications.



Ordering Information

Device Name	Package	Pins
iND88000	169-ball FC-CSP	7x7mm 0.50mm pitch
iND88002	196-ball FC-CSP	12x12mm 0.80mm pitch

iND880xx

Camera Video Processor

Four-camera Fully Independent and Configurable High Dynamic Range Image Signal Processor (ISP)

- Multi-channel 24-bit ISP
  - –Less than 1ms ISP processing latency
  - –Up to 1400 MPixel/second processing
  - –Supports up to 4 cameras with 8 independent contexts
  - –e.g. 4x 3MP60, 1x 16MP30, 2x 8MP60
- Advanced color filter array processing
  - –RGB-IR, RGGB, RCCB, RCCG, RYYCy, RCCC
  - –Optimized RGB-IR (4x4 only)
- High Dynamic Range (HDR) support
  - –144 dB HDR 24-bit pipeline
  - –2 and 3 exposure on-chip combiner
  - –Advanced Local Tone Mapping
- Simultaneous support for different frame rates, resolutions, and CFAs
- Advanced spatial (2D) noise reduction
- Zone-based statistics for AE and AWB
- Color noise reduction

eWARP Geometric Processor

- Proprietary 6th-gen eWARP® geometric processor
- Independently dewarps up to four 200+ degree videos
- Ultra-wide field of view (FOV) lens distortion correction
- Ultra-low latency (typically 1/6th of a frame)
- Dynamic Electronic Pan/Tilt/Zoom (ePTZ)
- Lens distortion, perspective, and alignment correction

Graphics Display Processor

- Scaling, compositing, blending, and surround
- 2D graphics engine supports 2x 1920x1080 at 60fps
- Tessellation engine for lines, quadratic and cubic Bezier curves
- Imaging and pixel engines for rendering and compositing
- Animated bitmap support

Dedicated Hardware Security Module and Safety Island

- Dual core lock step security, safety 800MHz 32-bit RISC processor
- Secure processing and memory environment
- Asymmetric/symmetric key and Hash cryptography
- Secure boot
- Key provisioning mechanisms
- True Random Number Generator (TRNG)
- Secure debug
- Signature verification on video input/output streams
- One Time Programming (OTP) memory

Dual 32-bit RISC Tensilica™ LX7 Microprocessor

- Operation up to 714 MHz
- Floating point and multiply/divide accelerators
- 32 KB Instruction cache/32 KB data cache per core

Video Inputs

- Dual 10 Gbps (4-lane @2.5Gbps/ lane) (MIPI D-PHY)
- Supports up to RAW24 and YUV 4:2:2-12
- 16 virtual channels per port

Video Outputs

- Dual 10 Gbps (4-lane @2.5Gbps/ lane) MIPI D-PHY or 17 Gbps (3xtrios @2.5Gbsps/ lane) MIPI C-PHY
- 8 Virtual channels on each transmit port
- Additional OpenLDI output interface
- Customizable embedded data in video stream
- Supports various RGB and YUV formats

System Interfaces

- Two SPI ports
- One Quad SPI (QSPI) SNOR for boot
- One 100/1000 RGMII
- Four Inter-Integrated Circuit (I2C™) ports (2x master and 2x slave)
- Dual CAN 2.0/CAN-FD ports
- Four UARTs

iND880xx

Camera Video Processor

- Three pulse width modulators (PWM)
- Sixteen dedicated GPIO/GPO
- JTAG port (IEEE Standard 1149.1-1990)

Safety Features

- Support for hostless safety designs with customizable failure recovery management
- Customizable safety pin for host assisted safety design
- ECC support for all processor code spaces
- Windowed Watch Dog Timer
- Power, reset, and clock management
- Process, voltage, and temperature sensors
- ISO 26262 ASIL-B

Electrical Specifications

- Core supply voltage: 0.8V ±5%
- I/O supply voltages: 1.8V and optional 3.3V ±5%
- PLL supply voltage: 1.8V ±5%
- MIPI supply voltage: 0.8V and 1.8V ±5%

Package

- 169-ball FC-CSP, 7mm x 7mm, 0.5mm pitch
- 196-ball FC-CSP, 12mm x 12mm, 0.8mm pitch

	iND88000	iND88002
Pixel Rate (max)	700 MP/s	1400 MP/s
MIPI Inputs (CSI-2)	1	2
CSI2 Input speed	1x 10 Gbps	2x 10 Gbps
MIPI Outputs (CSI-2 and DSI)	1	2
MIPI Outputs	1x C-PHY v1.2 or 1x D-PHY v1.2	2x C-PHY v1.2 or 2x D-PHY v1.2
Package Size, Pitch, Balls	7x7 mm^2, 0.5 mm, 169	12x12 mm^2, 0.8 mm, 196
OpenLDI	No	Yes
Gigabit Ethernet	Yes	Yes
PWM [1]	3	3
UART [1][2]	3	4
CAN/CAN-FD	2	2 [1]
GPIO [3] GPO	9 6	8 8
I2C	3	4
SPI	2	2

[1] Includes interfaces multiplexed on other pins;

[2] Includes 2 UART for debug console output;

[3] Excludes GPIO multiplexed on other pins